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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,000	01/16/2004	Edouard Ritz	PF030026	7921
24498 7590 10/23/2007 JOSEPH J. LAKS, VICE PRESIDENT THOMSON LICENSING LLC PATENT OPERATIONS PO BOX 5312 PRINCETON, NJ 08543-5312			EXAMINER CHIN, RICKY	
			ART UNIT 4157	PAPER NUMBER
			MAIL DATE 10/23/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/759,000

Applicant(s)

RITZ, EDOUARD

Examiner

Ricky Chin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_.

DETAILED ACTION

Claim Rejections - 35 USC § 102

- 1) The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English.

- 2) Claims (1-11) are rejected under 35 U.S.C. 102( e ) as being anticipated by Valmiki et al, US 6,636,222. (Hereinafter Valmiki).

Regarding claim 1, Valmiki discloses the same structural properties of an electronic apparatus (see "Summary of the Invention") comprising: a graphics memory storing a first and a second graphics object (for "graphics memory" and "pictures memory" refer to column 6, lines 11-19 of Valmiki);

an OSD processor generating a first digital stream representing the first graphics object; a pictures memory containing a picture and generating a second digital stream; a mixer able to mix the first digital stream and the second digital stream into a video signal; means for converting the second graphics object into picture data; means for

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writing the picture data to the picture memory (for “OSD processor” and “mixer” refer to column 5, lines 8-64 of Valmiki where graphics display system is OSD equivalent and video compositor is mixer equivalent. Furthermore, memory controller “reads and writes video graphics data to and from memory”. Memory controller is also described as having “two substantially similar SDRAM controllers, one primarily for the CPU and the other primarily for the graphics display system, while either controller may be used for any and all of these functions”).

Regarding claim 2, which further recites an electronic apparatus according to claim 1, comprising: means for detecting overlaps between the first and the second graphics objects generating an overlap cue (see column 13, lines 3-21 of Valmiki, which discloses “The graphics windows may be displayed such that they may overlap or cover each other, with arbitrary spatial relationships.”).

3. An electronic apparatus according to Claim 2, comprising: means for controlling the mixer, means for conversion and means for writing as a function of the overlap cue (see column 13, lines 3-55 of Valmiki.)

4. An electronic apparatus according to Claim 1, comprising: a video memory supplied by a decoder and linked to the mixer (see “Summary of the Invention” column 2, lines 15-25 of Valmiki.)

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5. An electronic apparatus according to Claim 1, wherein the video signal is transmitted to an output connector (See column 5, lines 1-5 of Valmiki, which discloses an "output for providing a video output signal.).

6. An electronic apparatus according to Claim 1, wherein the means for converting the second graphics object into picture data are a piece of software executed by a main controller (see column 5, lines 12-18 of Valmiki, which discloses "graphics data for display produced by any suitable graphics library software.).

7. An electronic apparatus according to Claim 1, in which the picture memory is a stationary picture memory (See "Background of the Invention" of Valmiki which discloses "may include graphics, text and video.") Graphics includes a stationary picture.

8. A process for generating a video signal, comprising the following steps: generation by an OSD processor of a first digital stream representing a first graphics object; conversion of a second graphics object into a picture; writing of the picture to a memory; generation of a second digital stream from the memory; (See Column 6, lines 11-29 of Valmiki, which discloses a memory controller that "reads and writes video graphics data to and from memory". Memory controller is also described as having "two substantially similar SDRAM controllers, one primarily for the CPU and the other primarily for the graphics display system, while either controller may be used for any and all of these

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functions”) mixing of the first digital stream and of the second digital stream; generation of a video signal from said mixture. (See column 6 lines 11-29 of Valmiki, which discloses a “graphics blender” that provides generation of a video signal from mixture. Anticipation and capability of performing said functions is clearly evident.)

9. A process for generating a video signal according to Claim 8, wherein said mixture is produced with application of a transparency coefficient. (refer to column 13, lines 11-64. “the display engine generates a pixel map accordingly and performs the blending in real time when the graphics window is to be displayed”).

10. A process for generating a video signal, comprising the following steps: reception of a command to display a first and a second graphics object; detection of a possible overlap between the first and the second graphics object; if absence of overlap, generation by an OSD processor of a digital stream representing the first graphics object and the second graphics object, and generation of a video signal based on the digital stream; if presence of an overlap: generation by an OSD processor of a first digital stream representing a first graphics object; conversion of the second graphics object into a picture; writing of the picture to a memory; generation of a second digital stream from the memory; mixing of the first digital stream and of the second digital stream; generation of a video signal from said mixture. (See column 17, lines 45-55 of Valmiki, which discloses, “Windows may be specified to overlap one another.”)

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11. Electronic apparatus comprising: an OSD processor managing an OSD plane; a mixer able to mix a picture plane and the OSD plane; means for converting a graphics object into picture data; means for writing the picture data to the picture plane.

See Claim 1.

### Conclusion

3) The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US Patent 6768774 teaches a Video graphics system with video scaling
2. US Patent 6744472 teaches a graphics display system with video synchronization feature
3. US Patent 6661422 teaches a video and graphics system with MPEG specific data transfer
4. US Patent 5838335 teaches a graphic data processing method and device
5. US Patent 4956707 teaches an adaptive graphics video standards format converter
6. US Patent 6005629 teaches a system for converting digital television signals
7. US Patent 5045946 teaches a method for multi-screen operation in a picture in picture system
8. US patent 6434097 teaches a digital video apparatus user interface
9. JP 11259057 teaches a graphics display system for use in computers

### Contact

4) Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ricky Chin whose telephone number is 571-270-3753. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on 571-272-7332. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
VU LE  
SUPERVISORY PATENT EXAMINER